Detector Support Group

Weekly Report, 2019-09-10

Summary

Hall A

- Cut and terminated 96 BNC to LEMO cables
  - ~70% completed

Hall A– GEM Gas Systems

- Created GEM Gas Distribution Rack diagrams including mass flow meters
- Continued development of 3D model for Gas Distribution system using NX12
  - Added pipe fittings/connectors to the pressure regulator and gauges

Hall A – Super BigBite Spectrometer (SBS) HCAL

- Cut 50 cables; removed 35 labels and stripped outer jackets and braid of 17 ends

Hall B – HDIce

- Troubleshooting USB to RS232/485 converters on the Windows 10 machine
  - Reinstalled missing NI-Serial driver
- Debugged RS485communications of the NMR rack
  - Added solder to fix bad ground connection in RF Box
  - Added property node for the RS-485 communication in the FRS program to change to 2-wire connection

Hall B – Magnets

- Increased EPICS PV array size to 4000 samples (from 2000) now that we're using 32-bit floats to improve DAQ timing
  - ADC still reading at 10 kHz; EPICS and PLC are being updated at 2.5 Hz

Hall B – RICH

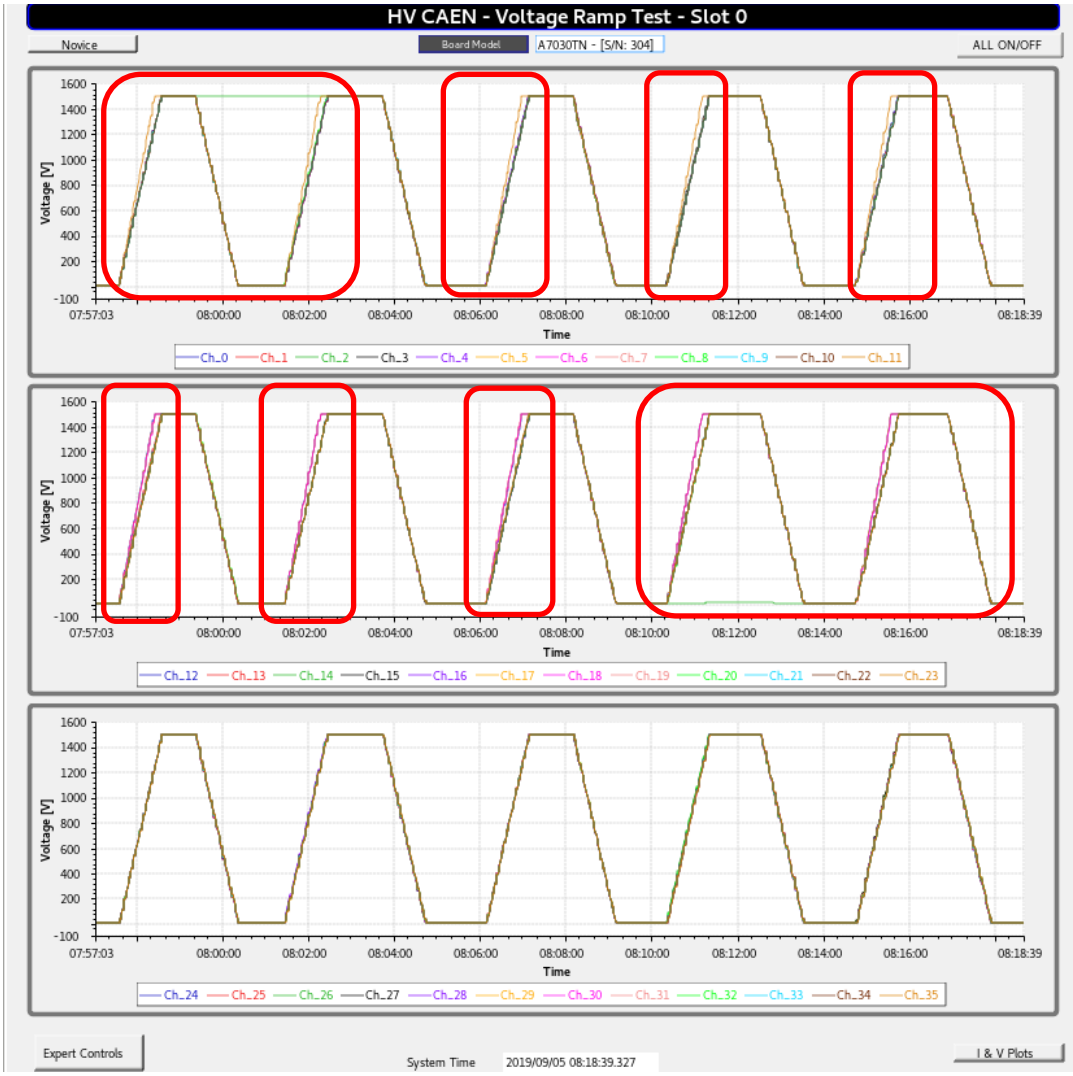
- Began development of d0 measurement program using LabVIEW
  - Program reads in data files and calculates d0
  - Program would be used to create consolidated d0 measurement program that runs on one PC for future RICH sectors
    - DAQ/analysis was done on Debian Linux PC and a Windows PC was used for stepper motor control in previous version

Hall B – SVT

- Recovered chiller fault (chiller tripped off first and cRIO was just reacting to that before tripping off): cleared interlocks and reset comms to the chiller

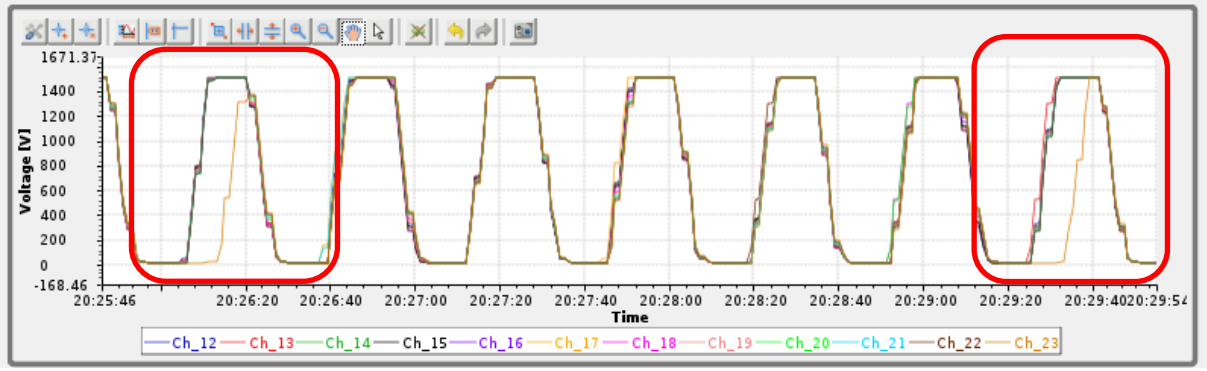
Hall C – CAEN HV EPICS Test Station

- Re-tested a single CAEN-A7030TN board using CSS-BOY screen for controls/monitoring and GECO 2020 for data logging
  - ✶ Conditions and specifications for the tests were the same as in previous tests (see Weekly Report 2019-09-03)
  - ✶ Only executed commands to power on/off channels and set parameters once
  - ✶ Noticed from the tests:
    - ▪ Channels randomly not turning on/off after JavaScript to turn on/off all 36 channels simultaneously was executed on HV CAEN Expert Controls CSS-BOY screen
    - ▪ Parameters of some channels randomly did not get set value on first attempt after executing the JavaScripts
    - ▪ All PVs kept initial set point values during tests
    - ▪ No discrepancies between GECO 2020 and EPICS PVs



Voltage Ramp Test—Slot 0 CSS-BOY screen shows test #1 results. Red rounded rectangles highlight the issues found

- Tested CAEN-A7030TN HV board using GECO 2020 Script advanced feature to control, and CSS-BOY screen to monitor, voltage
  - ✶ Conditions and specifications for the test were the same as for previous test (see Weekly Report 2019-09-03)
  - ✶ Noticed from this test:
    - Discrepancy between GECO 2020/SSH and EPICS PV for *Pw* parameter resolved after CSS-BOY screen is refreshed or *"camonitor"* EPICS command is re-executed
    - No other monitored PVs (Vmon, Vmax, Imon, etc.) had issues when EPICS command *"camonitor"* was executed once in the Host PC (EPICS client)
    - *Pw* PV readout for channel 23 had an update latency of ~8 s while ramping to set voltage; issue occurred twice and resolved itself in next cycles (see figures below)

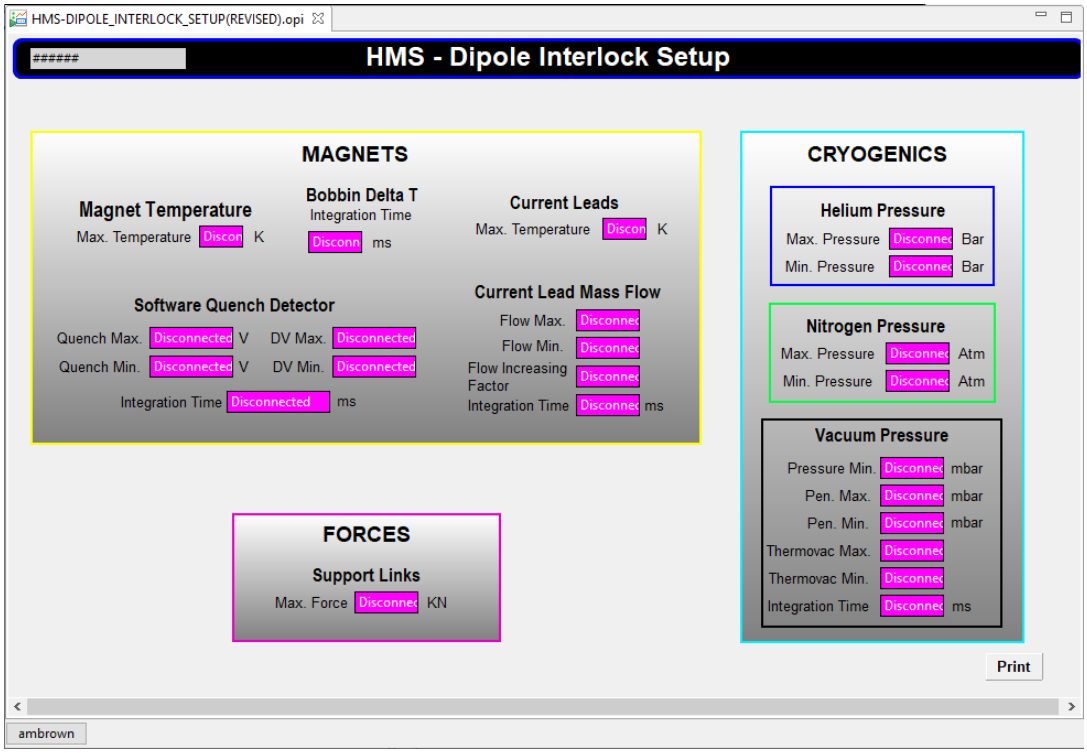


Zoomed view of *Voltage Ramp Test – Slot 0* CSS-BOY screen shows channel 23 ramped ~8 s later

- Detailed results for both tests sent to CAEN support

Hall C - EPICS

- Continued development of HMS magnets screens
  - ✶ Reorganized layout of *HMS Dipole Interlock Setup* CSS-BOY screen to improve functionality and visibility for future users



Revised CSS-BOY HMS Dipole Interlock Setup screen converted from FactoryTalk View for Hall C. This screen was revised to look more like the screens that have been previously converted and to add more information (like units) and improve functionality.

DSG R&D – cRIO Test Stands

- Made drawing of NI-9474 test wiring using Visio
- Wired NI-9203 module for testing
- Wrote and tested all manual tests (samples, differential nonlinearity, dynamic range, gain error, integral nonlinearity, and offset error)

DSG R&D – LV Chassis FPGA

- For the FPGA programming: installed Quartus (v.18.1) and SoCEDS software in *dsgtplc1-PC*
- Began development of LV cRIO's excitation program in C