Detector Support Group
Weekly Report, 2019-09-17

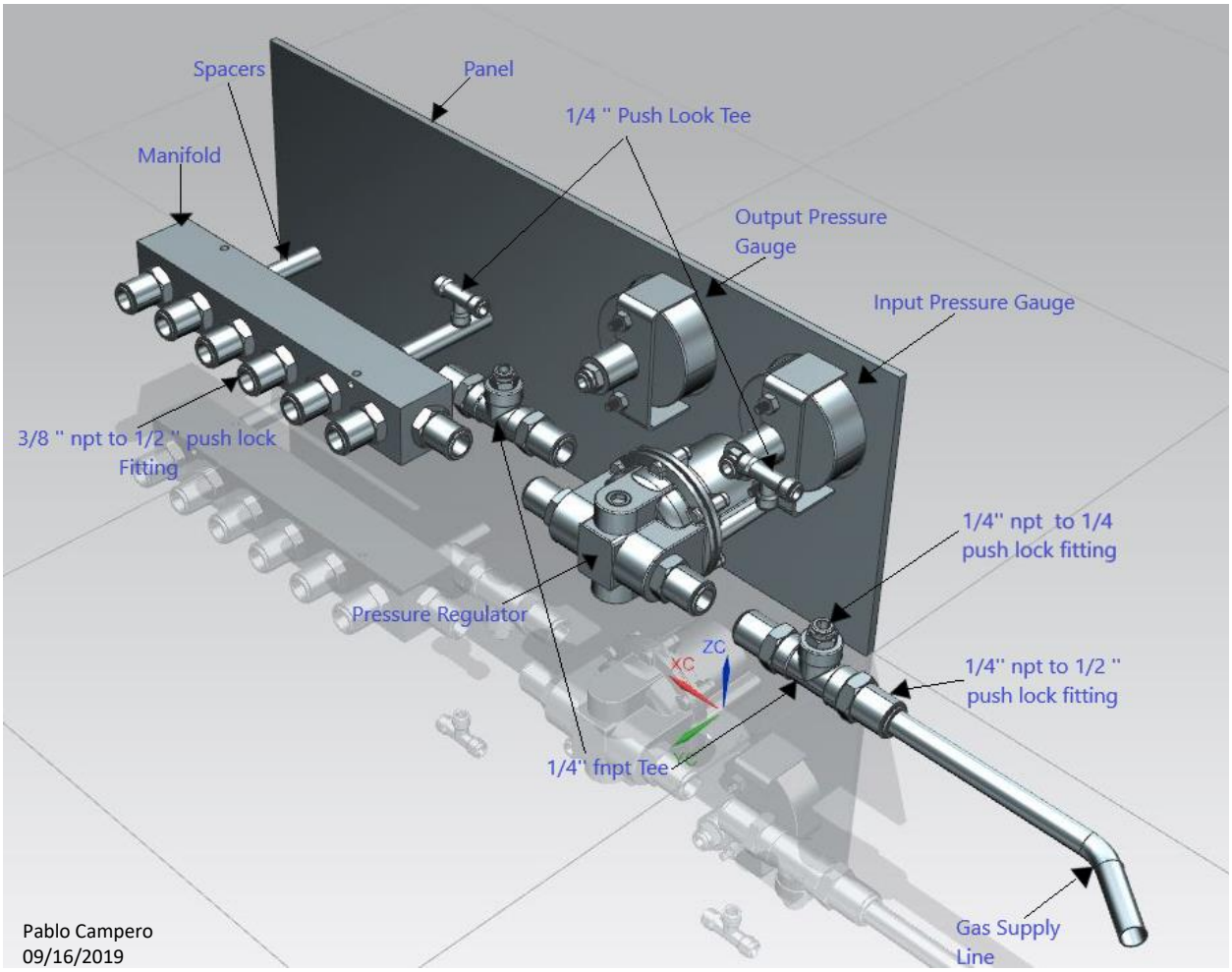
Summary

Hall A

- Terminated 112 BNC to LEMO cables
  - ~75% Completed

Hall A– GEM Gas Systems

- Honeywell sensor irradiated in Hall A during experimental run tested to verify that its performance didn't change after irradiation
  - Data analysis in progress; looks like little to no change from before
- Continued development of 3D model for Gas Distribution system using NX12
  - Added spacers to align manifold with pressure regulator



Hall A – Super BigBite Spectrometer (SBS) HCAL

- Cut 126 cables; removed 40 labels and stripped outer jackets and braid of 74 ends

Hall B – RICH

- Completed conversion of C analysis code to LabVIEW
  - ✶ LabVIEW calculates d0 to within 0.017 mm of original C program
  - ✶ Next step is to add Ximea CCD controls and image acquisition to the program

Hall C – CAEN HV EPICS Test Station

- Modification of CLAS6 HV Test chassis has started
  - ✶ Circuit wired to control 36 relays to work with cRIO
  - ✶ Relay coil control returns have been separated to work in groups of relays

Hall C - EPICS

- Continued development of HMS magnets screens using CSS-BOY
  - ✶ Compiled master list of completed screens (35) and updated the number of screens left to complete (238)

Accelerator Division R&D – Wire Bonding

- Ordered new wire
- Attempting to bond superconducting Nb3Sn sample

DSG R&D – cRIO Test Stands

- Made Visio drawing of NI 9203 test wiring
  - ✶ Completed automated test
- Developed digital input/output test for NI 9401 and NI 9402 modules
  - ✶ Input test uses FPGA to read a square wave of known frequency generated by an Agilent signal generator at 40 MHz and calculate period of input signal
  - ✶ Output test uses Tektronix oscilloscope to measure frequency of FPGA generated output signal
  - ✶ Input/output frequencies tested: 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz

DSG R&D – LV Chassis FPGA

- Working on integrating current LV FPGA code with SoC
  - ✶ Code compiles, puts serial data in memory, but trying to access it from Linux causes freezes
- Installed *Altium Designer* software in *dsgtest1*-PC to analyze printed circuit boards located inside LV chassis
- Configured and installed *USB-Blaster II* to connect Altera FPGA board to *dsgplc1* PC via USB

DSG R&D – PLC Test Station

- To develop new HMI alarm screen for test station, debugged communication issues between CompactLogix L35E PLC controller (Firm. Rev. 20) and FactoryTalk View rev. 8
  - ✶ Installed Ethernet board in *dsgwin10* PC to replace RS-232 serial connection with Ethernet TCP/IP