Detector Support Group

We choose to do these things "not because they are easy, but because they are hard".

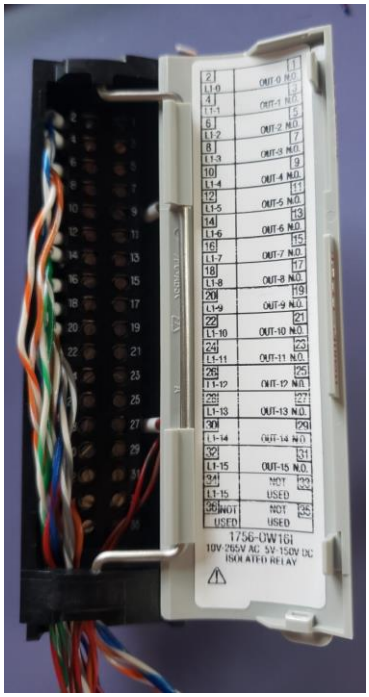
Weekly Report, 2021-09-22

Summary

Hall A – SoLID

Mary Ann Antonioli, Pablo Campero, Brian Eng, Mindy Leffel, Marc McMullen

- Generating PLC code to simulate PID control over the valves
    - ✶ Modified code to add function block diagram subroutine
    - ✶ Configured controller properties in PLC program to connect with emulator
- Modifying Instrumentation Rack AutoCAD layouts based on power distribution changes
    - ✶ Added 5 VDC power supply for radial and axial load sensors
- Fabricated five 20-conductor ferrule-to-ferrule cables
- Wiring Allen Bradley terminal blocks; five of 13 complete



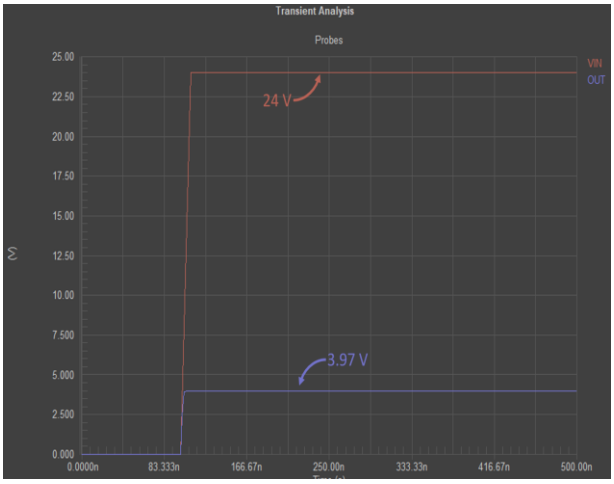
Wired Allen Bradley terminal block

- Generated spreadsheet detailing connections between terminal strips and PLC IO module's terminal block

Hall B – RICH-II

Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen

- Simulated RMC's Schottky diode circuit in Altium
    - ✶ Voltage input was a 24 V step
    - ✶ Simulation shows that while the voltage input to the circuit can be large, the voltage level at device will stay at ~4 V



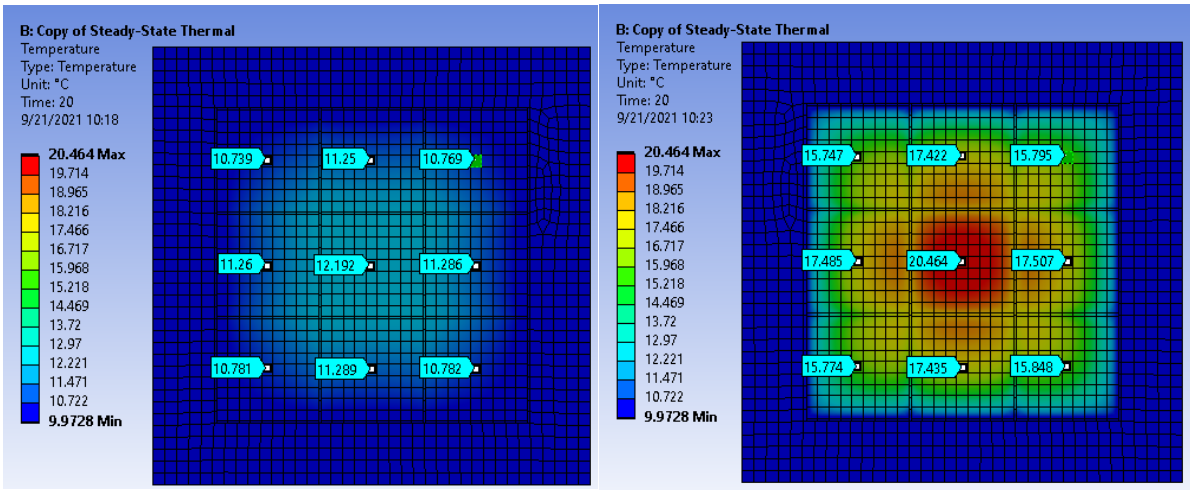
Output of Altium simulation

- Prepared equipment for d0 measurements of spherical mirrors
  - ✶ Set up linear stages and Debian PC in cleanroom; connected instrumentation

Hall C – NPS

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Conducted simulation of two 5 cm sections of 3x3 blocks of $PbWO_4$ crystals
  - ✶ One section represents the front 5 cm of the full 20 cm crystal, the other section represents the back 5 cm
  - ✶ This was done in an effort to understand why the temperature profiles of the front and rear faces of the crystals are nearly identical
- Conducted simulation of 3x3 block of full length (20 cm) crystals
  - ✶ Increased heat load to 5 W to see how that affected the temperature profiles of front and rear crystal faces

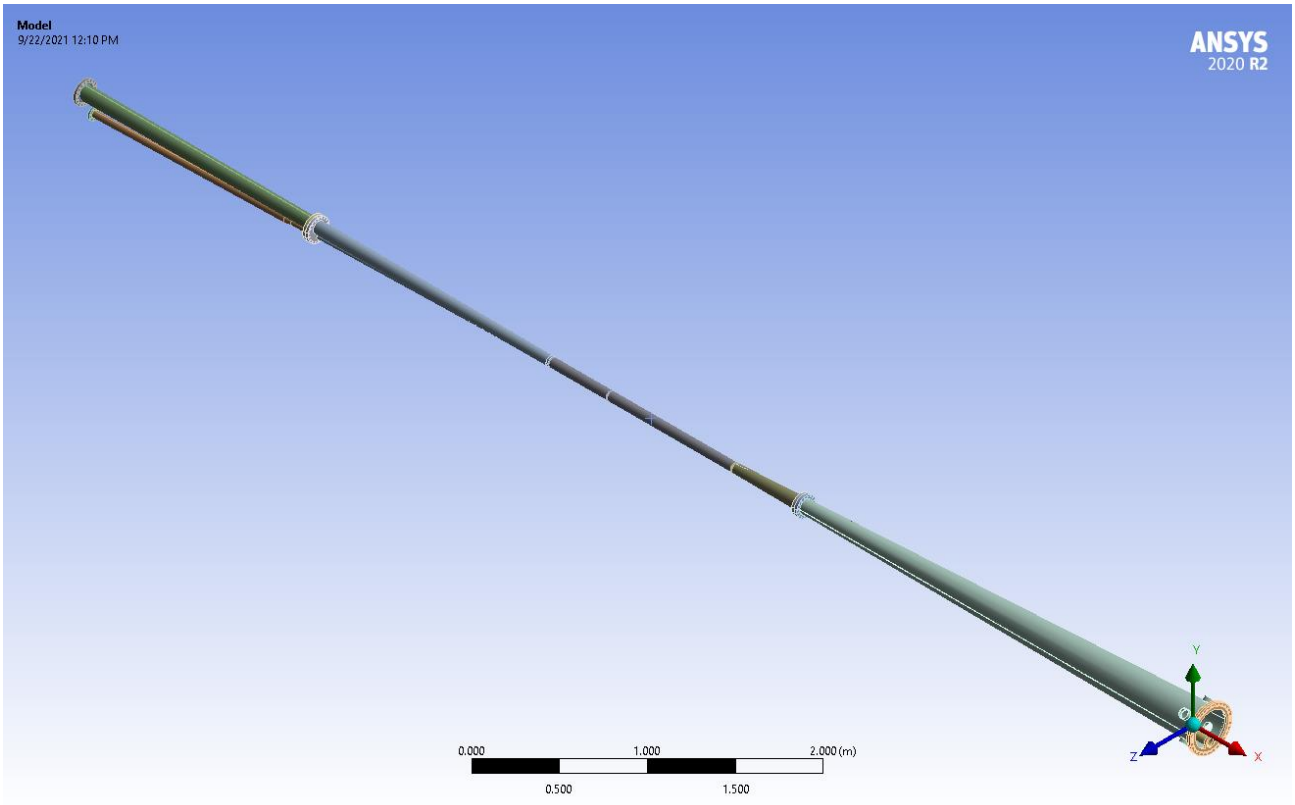


Screenshots of front (left) and rear (right) faces of the full length crystals; maximum temperature was ~20°C

EIC

Pablo Campero, Brian Eng

- Starting Ansys thermal analysis of beam pipe and Si tracker – researching material properties



Screenshot of Ansys beam pipe model

- Attended ATHENA tracking working group meeting
  - ✶ Changing disk tracking design (silicon disks inside of MPGD disks)

DSG R&D – NPS

Peter Bonneau

- Researched the readout and control of the Keysight switch/measurement unit using Python
  - ✶ A library of command sequences specific to the Keysight mainframe and the multiplexer would be developed using the *PyVISA* Python package
  - ✶ The *PyEpics* package could be used to interface the mainframe's DAQ program to an EPICS-based CS-Studio Phoebus display which could also be generated using Python